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NOVELICS CORPORATION OVERVIEW

Aliso Viejo, CA — October 11, 2006 — Novelics a memory IP provider for versatile and differentiated memory IPs, today announced its entry in the IP market, with the specific focus of providing low power memory blocks to be used by fabless semiconductor, SOCs, ASSP, and ASIC designers.

Founded in July 2005, Novelics comprises a team of seasoned engineering and management professionals whose backgrounds represent the convergence of three key areas: embedded memory volatile/non volatile memory (NVM) architectures, compiler design and custom low power design. Novelics's management has more than 60 man-years of combined industry experience. Moreover, Novelics's track record of having many patents in their names and 9 pending since funding Novelics, as well as the depth and breadth of experience provided by the industry veterans on the company's technical and business advisory boards further enhance the technical expertise of the team.

“Novelics was conceived with one primary purpose in mind,” said Cyrus Afghahi, Co-founder and CEO of Novelics. “Our mission is to revolutionize ‘cool’ embedded memory to achieve the best value for power, density, speed, reliability and cost.

To enable fabless designers to break away from the trap created by huge cost adder for extra masks and lack of portability architectural breakthrough in design and automation was required. We

have amassed an extraordinary team of engineers whose combined expertise in circuit design, modeling, compiler design, reliability, manufacturability, BIST/ BISR for repair, low power architectures that will enable designers to implement their designs while they trade off power, density, reliability, performance, and cost,” Afghahi.

“The coincidence of the potential to address convergence in consumer space and create multi-million-gate designs with over 50% memory which is today’s norm, is creating a plethora of explosive market opportunities,” said Farzad Zarrinfar, member of advisory board at Novelics. “The trick is to use MemQuest™ the world’s first memory compiler for VM and NVM memory to perform tradeoff analysis and achieve design goals. We believe that customers would rather to negotiate with single supplier of differentiated IPs which is generated by MemQuest. Thus, wherever embedded memory finds their way into fabless designs, Novelics enable the designer to extract the maximum performance with the least amount of design time, power dissipation, and cost.”

Process and Technology Experience

Novelics has experience with over 10 different sub-micron processes including 0.25um, 0.18um, 0.13um, and 90nm feature processes. While other memory compiler have focused on developing generic least common-denominator libraries, Novelics memory design and MemQuest compiler takes full advantage of custom design methodology with lowest power, highest performance and density on that process. In addition to bulk CMOS logic process technologies, Novelics has experience with EEPROM, FLASH, DRAM memory processes and design architectures.

EDA Tools & Interoperability

Novelics is interfacing very closely with leading EDA tool vendors to provide views that match all leading edge tools. Novelics has developed an interoperability and verification

methodology to insure that highest quality for electrical, physical, simulation (Verilog & VHDL), synthesis tools.

Management Experience

Cyrus Afghahi, Ph.D. - CEO & Co-Founder

Dr. Afghahi received his Ph.D. from Linkoping University in Sweden and 26 years of general management and technical leadership. Mr. Afghahi was technical director for the office of the CTO at Broadcom, Principal Engineer at Intel, Head of R&D group at Ericsson Radio, Manager at SAAB electronic. He holds many patents and the author of many articles

Esin Terzioglu, Ph.D. - CTO & Co-Founder

Dr. Terzioglu received his Ph.D. from Stanford University. He has over 7 years of principal engineering at Broadcom, and Micron Technology. He holds many patents and the author of many articles.

Gil Winograd, Ph.D. - Chief Engineering Officer & Co-Founder

Dr. Winograd received his Ph.D. from Stanford University. He was Principal Engineer for 6 years at Broadcom. He holds many patents and the author of many articles.

About Novelics

Novelics, headquartered in Aliso Viejo, California, supplies a portfolio of innovative embedded memory IPs for low power, and high performance ASICs, ASSPs, and SOC designs. Our compiler-driven 'Cool' and 'zero-leakage' Memory IPs include OTP, SRAM-1T, SRAM-6T, high Speed Cache, and ROM.

These differentiated memory IPs are implemented with standard logic CMOS process with no additional masks or process steps to minimize cost, as well as maximize reliability and portability.

Our customers compete in low power consumer, industrial, wireless Applications, high speed computing and Networking. For more information, please visit www.novelics.com or email a request to 'info@novelics.com'.

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